Reduction of DC-link Ripples for SiC-based Three-phase Four-wire Inverters with Unbalanced Loads

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Abstract--- Three-phase inverters are widely used in the smart grid to integrate renewable energy resources. When the inverters are used to feed the unbalanced three-phase loads, the three-phase four-wire inverters are usually required to provide the current path for neutral currents. However, unbalanced loads will cause undesirable second-order ripples on DC bus. Conventional three-phase four-wire inverters with neutral legs can not address this challenge. Bulky capacitors or extra active circuits are still required to reduce the ripples. This inevitably leads to increased size and cost of the system. Although SiC-based converters have the advantage of achieving high power density, the DC-bus capacitance can not be reduced by simply replacing Si IGBTs with SiC MOSFETs. In this paper, a new topology of SiC-based three-phase four-wire inverters is proposed to reduce the DC-bus ripples without adding any additional hardware components. With the reduction of DC-bus ripples, the DC-bus capacitance can be reduced to achieve high power density. The equivalent circuit is analyzed and the control strategy for the proposed topology is designed. The proposed topology is built in Matlab/Simulink and simulation results are presented to verify the proposed topology.

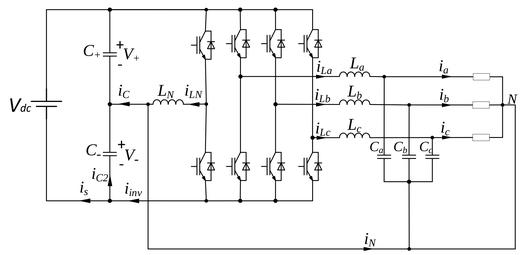

Fig. 1 A conventional topology of three-phase four-wire inverters.

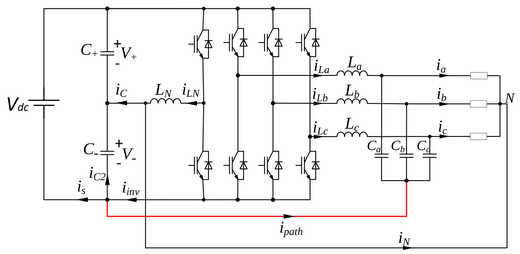

Fig. 2 Proposed Topology.

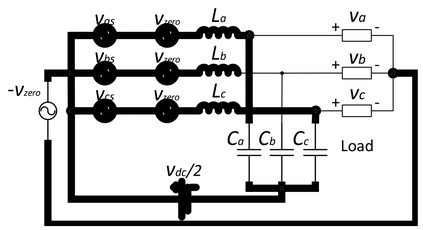

Fig. 3 Equivalent circuits of proposed topology.

Table I
SIMULATION PARAMETERS.

V_{dc}	800V	V_{ac_rms}	230V
Split DC capacitors	20 μF	Filter capacitors	20 μF
Neutral inductor	2.5 mH	Filter inductors	2.5mH
Switching frequency		20 kHz	
Load resistors	$R_a = R_b = 40\,\Omega$, $R_c = 160\,\Omega$		

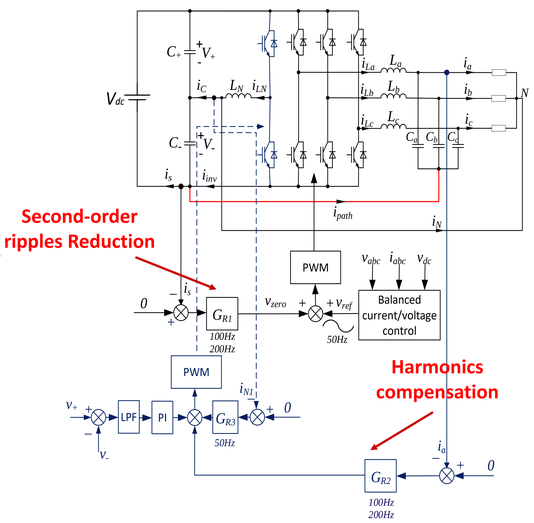

Fig. 4 Proposed control diagram.

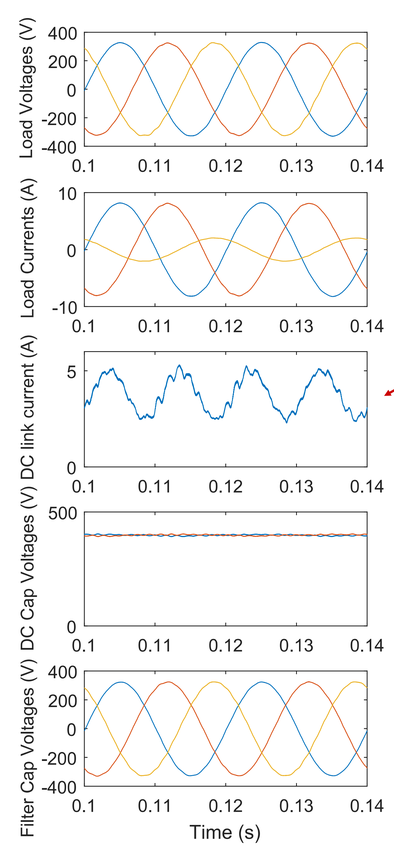

Fig. 5 Simulation results of conventional topology.

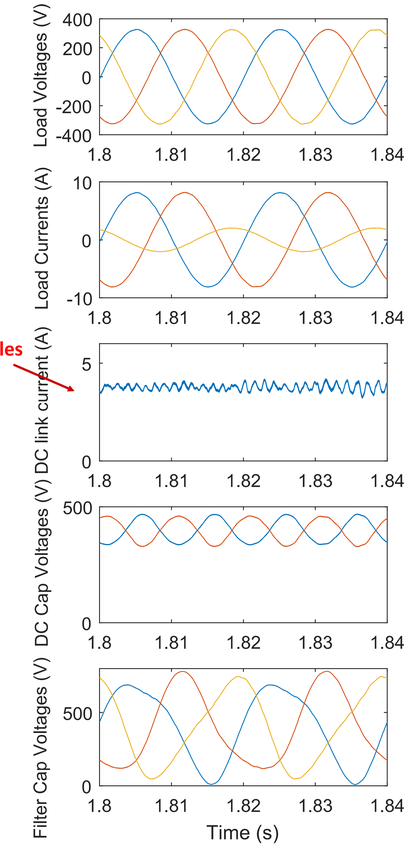

Fig. 6 Simulation results of proposed topology.

Conclusion

In this paper, a SiC-based three-phase four-wire inverter has been proposed to reduce the second-order ripples on the DC bus to achieve high power density. An additional conduction path is constructed between the negative DC bus and the AC filter capacitors. With the proposed control strategy, the second-order ripples are absorbed by the filter capacitors and the DC-bus ripples and capacitance are reduced. The above function has been achieved without adding any additional hardware components. It is also discussed that the proposed topology requires higher DC-bus voltage and causes higher current and voltage stress. The future work is to build the experimental testbench based on SiC MOSFETs to validate the proposed topology and analyze the efficiency of the converters.

Acknowlegment

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